

A Literature Survey of FPGA Implementation of Inverter Techniques

Rahul Patel (M.Tech student)

Department of Electronics and Communication
SSSUTMS University, Sehore, India
rp143hp@gmail.com

Prof. Vijay Prakash Singh (Asst. Prof.)
Department of Electronics & Communication Engineering
SSSUTMS University, Sehore, India
vijayprakash5478@gmail.com

Abstract— This paper reviews state of the art of multilevel inverter topologies using FGPA technology. Power electronics devices are which converts DC power to AC power at required output voltage and frequency level is known as inverters. Multilevel inverter has three different major topologies have been applied in industrial applications: Cascaded H-bridges converter, Diode clamped, and Flying capacitor multilevel inverter. This paper presents a review on various types of multilevel inverter (MLI) FPGA implementation. For the implementation of MLI using two type of phenomena in VHDL, the first one is CPLD and the second one is FPGA. FPGA is more popular as compare to CPLD now a days. In this survey paper give the brief over view of multi-level inverter (MLI) and different technique of MLI.

Index Terms— Multilevel inverter, PWM, FPGA, CPLD and VHDL

I. INTRODUCTION

Most analogue implemented PWM-control schemes have been based upon “natural” sampled switching strategies. More recently; a new switching strategy referred to as “regular sampling”, has been proposed which is considered to have a number of advantages when implemented using digital techniques. Since both natural and regular sampling techniques can be implemented using microprocessor technology, and are therefore likely to form the basis of most microprocessor PWM control.

The heart of any PWM control scheme is undoubtedly the switching strategy used to generate the switching edges of the PWM control waveform. It is possible by surveying the literature over the last decade to trace the historical development of PWM switching techniques and relate these developments to changes in technology starting from analogue-based systems through discrete digital, and more recently ROM-based and microprocessor-implemented controls schemes. [1]

II. FIELD PROGRAMMABLE GATE ARRAY (FPGA)

FPGAs are an efficient hardware for rapid prototyping. Its functions are complex enough to implement more than glue

logic. As the logic capacity of the FPGAs increases, synthesis for PGA is becoming more important. One solution to designing large designs efficiently is to use VHDL synthesis. Xilinx Field Programmable Gate Array (FPGA) is a user programmable device. [1]

III. XILINX FPGA PWM GENERATOR

FPGA is a Programmable Logic Device developed by Xilinx, Inc. It comprises of thousands of logic gates. Some of them combined together to form a Configurable Logic Block (CLB). CLB simplifies higher-level circuit design. Gates interconnections using software are defined through SFL4M or ROM. This provides flexibility to modify the designed circuit without altering the hardware pan. Concurrent operation, less hardware, easy and fast circuit modification comparatively low cost for a complex circuitry and rapid prototyping make it as the most favorable choice for prototyping an ASIC. [1]

IV. LITERATURE REVIEW

A. S. Mekhilef, A. Masaoud, “Xilinx FPGA Based Multilevel PWM Single Phase Inverter”, 2006

Summary- In this paper a XILINX FPGA based multilevel PWM single-phase inverter was constructed by adding a bi-directional switches to the conventional bridge topology. The inverter can produce three and five different output voltage levels across the load. XILINX FPGA is a programmable logic device developed by XILINX which is considered as an efficient hardware for rapid prototyping. It is used as a PWM generator to apply the appropriate signals to inverter switches. In addition to XILINX FPGA, Matlab/Simulink software was used for simulation and verification of the proposed circuit before implementation, Simulation and experimental results show that both are in close agreement.

The switching patterns adopted are applied at the six inverter switches to generate five or three output voltage levels at different modulation indexes. XILINX FPGA enables to make easy, fast and flexible design and implementation. The experimental and simulated results are show satisfactory results in term of total harmonic distortion and output voltage and current waveform shapes. [2]

B. Karuppanan P, AyasKanta SWAIN, KamalaKanta Makapatra, "FPGA Based Single-Phase Cascaded Multilevel Voltage Source Inverter Fed ASD Applications", 2008

Summary- This paper presents Field Programmable Gate Array (FPGA) based Sinusoidal Pulse Width Modulation (SPWM) controller for single-phase cascaded multilevel inverter fed Adjustable Speed Drive (ASD) applications. The cascaded inverter is constructed using three conventional full H-bridges for a seven-level output that reduces the harmonic content. PWM Voltage Source Inverter (VSI) should maintain the variation of both voltages and frequency simultaneously and keep their ratio constant for the control of speed. In this investigation, a simple SPWM control circuit is adopted using FPGA device. It can be accommodated in a single chip that provides high computation speed and accurate control signals for higher output voltages and currents with less harmonics. VHDL language is used to model the inverter switching strategies. The proposed controller generates 12-control switching signals that cascaded multilevel inverter for 7- level output voltage. Matlab/System generator and ISE/XILINX tools are used with hardware-co-simulation to synthesize the digital control architecture and the obtained architecture I embedded in FPGA.

The sinusoidal PWM technique is adopted with FPGA to generate switching patterns. These switching pulses are applied to the cascaded multilevel inverter to generate 7-level output voltage. This controller design is simulated and compilation portion is tested through FPGA in real time process using hardware-co-simulation. FPGA enables easy, fast and flexible implementation of the controller circuit in hardware. It can adjust effectively the modulation index range for varying speed control of induction motor drive. The effective controller maintains the voltage to frequency ratio constant. The simulation with experimental results demonstrates quality of voltage and current waveforms with less harmonic content at the output of the cascaded inverter. These inverter topologies with digital-control circuit can be used for speed control of induction motor and other medium scale industrial applications. [3]

C. Jagdish Kumar, Biswarup Das, Pramod Agarwal, "Harmonic reduction technique for a cascade multilevel inverter", 2009

Summary- In this research, an optimization technique is proposed to calculate the switching angles to the fundamental frequency of switch system by solving nonlinear transcendental

equations (known as selective harmonic elimination equations), thus eliminating certain harmonics predominating lower order, and at the same time, control over the magnitude of the output voltage of a multi-level inverter is reached. Since these equations are nonlinear transcendental in nature, there may be a simple, multiple or even for a particular value of a modulation index. The proposed scheme is implemented so that all possible solutions are obtained without knowing the proper initial estimate solutions. Moreover, this technique is suitable for the high level of multilevel inverters where other existing methods fail to calculate switching angles due to more computational load. For values of modulation indices for which there are many solutions, the solutions that produce less THD in the output voltage is selected. A significant decrease DHT is obtained by considering several sets of solutions instead of taking a single set of solution. Calculation results are displayed graphically for better understanding and proving the effectiveness of the method. An experimental 11-level multilevel cascade inverter is used to validate the results of calculation. [4]

D. Jin Wang, Damoun Ahmadi, "A Precise and Practical Harmonic Elimination Method for Multilevel Inverters" 2010

Summary- Multilevel inverters have been widely used in applications in medium and high voltage. Selective Harmonic Elimination for voltage waveform generated by the staircase multilevel inverter has been widely studied in the last decade. Most methods published on this subject were based on solving multivariate groups of high order polynomial equation from the Fourier series expansion. This research presents a different approach, which is based on criteria of equal and harmonic injection area. With the proposed method, regardless of the number of voltage levels are involved, only four simple equations are needed. The results of a case study, with a maximum of five switching angles show that the proposed method can be used to achieve excellent removal performance of the harmonics of the modulation index range of at least 0, 2 to 0.9. To demonstrate the adaptability of the proposed method for waveforms with a high number of switching angles, experimental results on a 1-MVA 6000 V-17 level cascaded multilevel inverter are also presented to the end of this research. [5]

E. Swamit S. Tannu Dr. R. R. Sawant Dr. Y. S. Rao, "Discrete Time Control Technique for Induction Heating System", 2012

Summary- A novel discrete time control technique for Induction heating system is discussed. Discrete time control system is modular and flexible compared to its continuous counterpart. This control system holds major advantages of both phase shift control and pulse density modulation. Complete performance analysis of newly developed algorithm was done by conventional load simulations and Hardware in Loop Simulation (HILS). Superior to conventional control

technique this technique enables us to implement configurable control system over an embedded processor.

Complete discrete time control technique was developed for VS-SRI based induction heating system. Control technique was validated by simulating different load scenarios. It is observed that algorithm successfully regulates the power without losing ZVS over a wide range of load variations. It is possible to implement this algorithm in embedded processor since algorithm demands commercially feasible sampling rates even at very high resonance frequencies. [6]

F. M. Mythili, N. Kayalvizhi, "Harmonic Minimization in Multilevel Inverters Using Selective Harmonic Elimination PWM Technique" 2013

Summary- In general, the inverter output voltage must be sinusoidal. However, the waveforms of the inverters practical non-sinusoidal and contain certain harmonics. For low and medium power applications, square wave or quasi-square wave may be acceptable, but for high power applications, low distorted sinusoidal waveforms are required. By number of levels in the UPS by increasing the output voltage has several steps generating a form of stairs, which reduces harmonic distortion. Emerges need a multi-level inverter. In this cascade research work multilevel inverter with selective removal of Pulse Width Modulation harmonics (SHE-PWM) technique is implemented. The SHE-PWM problem is to solve the non-linear transcendental equations that are used to determine the switching angles. Here the evolutionary algorithm based on natural selection is proposed to solve the equations that reduce the computational load resulting from the faster convergence. The main benefits are reduced total harmonic distortion and low switching frequency. To validate the results of calculation for the switching angles, a simulation is performed in the MATLAB / Simulink software tool for a level 7 cascade H-bridge inverter. [7]

V. CONCLUSION

This paper presents a brief review of various inverter techniques. Here main objective of this review paper is to focus on multilevel inverters. We conclude various multilevel inverter techniques also review previously done work.

REFERENCES

- [1] Saad MeHulef, N. A. Rahim, "Xilinx FPGA Based Three-Phase PWM Inverter And Its Application For Utility Connected PV System", Proceedings of IEEE TENCON 2002.
- [2] S. Mekhilef, A. Masaoud, "Xilinx FPGA Based Multilevel PWM Single Phase Inverter", Electronic Journal of University Malaya (EJUM), Vol.1, No 2 December 2006 pp. 40-45.
- [3] Karuppanan P, AyasKanta SWAIN, KamalaKanta Makapatra, "FPGA Based Single-Phase Cascaded Multilevel Voltage Source Inverter Fed ASD Applications", Journal of Electrical Engineering, 2006.
- [4] Jagdish Kumar, Biswarup Das, and Pramod Agarwal, "Harmonic reduction technique for a cascade multilevel inverter" International Journal of Recent Trends in Engineering, vol.1, no. 3, May 2009.
- [5] Jin Wang and Damoun Ahmadi, "A precise and practical harmonic elimination method for multilevel inverters" IEEE Transactions on Industry Applications, vol. 46, no. 2, pp. 857-865, March/April 2010.
- [6] Swamit S. Tannu Dr. R. R. Sawant Dr. Y. S. Rao, "Discrete Time Control Technique for Induction Heating System", IEEE, International Conference on Communication, Information & Computing Technology (ICCICT), Oct. 19-20.
- [7] M. Mythili, N. Kayalvizhi, "Harmonic Minimization in Multilevel Inverters Using Selective Harmonic Elimination PWM Technique", 2013 International Conference on Renewable Energy and Sustainable Energy [ICRESE'13], IEEE 2013.